Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for optimizing body bias connections in a CMOS circuit substrate using a deep n-well grid structure, said method comprising:

performing a layout for said deep n-well grid structure which routes body bias voltage and which is buried at least a first depth below a surface of said CMOS circuit substrate;

determining an isolation region, and a connection region for placing body biased n-wells;

prioritizing a plurality of PFETs for placement in said body biased n-wells; and

performing a circuit layout wherein the plurality of PFETs are placed in the CMOS circuit wherein a subset of said plurality of PFETs are placed in the body biased n-wells in accordance with said prioritizing.

2. (Original) The method of Claim 1, wherein said deep n-well grid structure comprises an aperture that is approximately square with a dimension of substantially 7 microns.

3. (Original) The method of Claim 1, wherein the layout of the deep n-well grid structure is performed independently from the circuit layout.

4. (Original) The method of Claim 1, wherein the prioritizing is performed on the basis of inclusion on a critical path.

5. (Original) The method of Claim 1, wherein the prioritizing is performed on the basis of power dissipation

6. (Original) The method of Claim 1, wherein the prioritizing is performed on the basis of the effects of leakage current anticipated by modeling of the plurality of PFETs.

7. (Original) The method of Claim 1, further comprising determining a buffer region for separating said connection region and said isolation region.

8. (Currently Amended) A method for optimizing body bias connections in a CMOS circuit substrate using a deep n-well grid structure, said method comprising:

performing a layout for said deep n-well grid structure which routes body bias voltage and which is buried at least a first depth below a surface of said CMOS circuit substrate;

determining an isolation region, and a connection region for placing body biased n-wells;

prioritizing a plurality of PFETs for placement in said body biased n-wells; and

performing a circuit layout wherein the plurality of PFETs are placed ~~in the body biased n-wells~~ in one of said isolation region and said body-biased n-wells of said connection region in accordance with said prioritizing of the PFETs.

9. (Original) The method of Claim 8, wherein said deep n-well grid structure comprises an aperture that is approximately square with a dimension of substantially 7 microns.

10. (Original) The method of Claim 8, wherein the grid layout is performed independently from the circuit layout.

11. (Original) The method of Claim 8, wherein the prioritizing is performed on the basis of inclusion on a critical path.

12. (Original) The method of Claim 8, wherein the prioritizing is performed on the basis of power dissipation.

13. (Original) The method of Claim 8, wherein the prioritizing is performed on the basis of the effects of leakage current anticipated by modeling of the PFETs.

14-35. (Canceled)